ELEC2141
DIGITAL CIRCUIT DESIGN

Course Outline – Semester 1, 2015

Never Stand Still | Faculty of Engineering | School of Electrical Engineering and Telecommunications

Course Staff

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Consultations: You are encouraged to ask questions on the course material, after the lecture class times in the first instance, rather than via email. Lecturer consultation time is on every Wednesday 11am-12pm. ALL email enquiries should be made from your student email address with ELEC2141 in the subject line, otherwise they will not be answered. You are also encouraged to post questions related to the course syllabus on the Moodle discussion forums. Such questions will be addressed by the lecturer, other course staff and fellow students.

Keeping Informed: Announcements may be made during classes, via email (to your student email address) and/or via online learning and teaching platforms – in this course, we will use Moodle https://moodle.telt.unsw.edu.au/login/index.php. Please note that you will be deemed to have received this information, so you should take careful note of all announcements.

Course Summary

Contact Hours

The course consists of 3 hours of lectures, a 1-hour tutorial, and a 2-hour laboratory session each week. Tutorial and laboratory classes will start in week 2 and week 4, respectively.

Lectures	**Day**	**Time**	**Location**
	Wednesday	4pm – 6pm	Ritchie Theatre
	Thursday	1pm - 2pm	Colombo Theatre A
Tutorials	Monday	12pm – 1pm	Gold G16
	Tuesday	5pm – 6pm	Gold G16
	Wednesday	9am-10am	Webst 256
	Wednesday	10am – 11am	Webst 256
Laboratories	Monday	1pm-3pm	EE233
	Tuesday	1pm-3pm	EE233

	Tuesday	3pm-5pm	EE233
	Wednesday	11am-1pm	EE233
	Wednesday	1pm-3pm	EE233
	Wednesday	3pm-5pm	EE233
	Thursday	9am-11am	EE233
	Thursday	11am-1pm	EE233
	Friday	9am-11am	EE233
	Friday	11am-1pm	EE233

Context and Aims

Digital circuits are integral parts of many areas of engineering and technology such as personal computers, digital signal processing, telecommunications, speech analysis and recognition, and control systems. The objective of this course is to equip students with the necessary fundamental knowledge and skill that enable them to understand, analyse and design digital circuits in the real world. The first half of the course will focus on the analysis and design of combinational and sequential logic circuits. Verilog Hardware Description Language, arithmetic circuits, computer design fundamentals and CMOS and TTL technologies will be covered in the second half of the course. At the completion of the course, students should be in a position to be able to design and build reliable and cost-effective digital circuits.

The course aims to provide students with fundamental knowledge of digital systems with respect to several different levels of abstraction – from a low-level dealing with electrical circuits through to a high-level dealing with software tools and hardware description languages.

Indicative Lecture Schedule

Period	Summary of Lecture Program
Week 1	Introduction to digital systems and number systems
Week 2	Combinational logic circuit analysis I
Week 3	Combinational logic circuit analysis II
Week 4	Combinational logic circuit design
Week 5	Sequential circuit elements
	Break
Week 6	Sequential circuit analysis **Assignment I due**
Week 7	Sequential circuit design
Week 8	Verilog HDL I
Week 9	Verilog HDL II
Week 10	Arithmetic Circuits
Week 11	Computer design fundamentals **Assignment II due**
Week 12	Digital logic families and CMOS technology

Indicative Laboratory Schedule

Period	Summary of Laboratory Program
Week 4	Introduction to digital circuits
Week 5	Introduction to Xilinx ISE and Digilent Nexys
	Break
Week 6	Comprehensive Guide to FPGA Programming
Week 7	Combinational circuit design
Week 8	Flip-Flop Basics
Week 9	Sequential circuit design
Week 10	Counters and 7-segment display
Week 11	Electronic handball game design
Week 12	Catch up lab
Week 13	**Lab Exam**

Assessment

Fortnight online quizzes	5%
Laboratory Practical Experiments	15% (+5% bonus +2% optional labs)
Lab Exam	5%
Assignments (I & II)	15%
Final Exam (3 hours)	60%

Course Details

Credits

This is a 6 UoC course and the expected workload is 10–12 hours per week throughout the 13 week semester.

Relationship to Other Courses

This is a 2nd year course in the School of Electrical Engineering and Telecommunications. It is a core course for students following a BE (Electrical) or (Telecommunications) program.

Pre-requisites and Assumed Knowledge

The pre-requisite for this course is ELEC1111(2): Electrical and Telecommunications Engineering, which introduced basic concept of electrical circuits. It is further assumed that you have a good computer literacy

Following Courses

The course is a pre-requisite for ELEC2142: Embedded Systems Design, in which the digital system design concepts introduced in ELEC2141 will be applied extensively. It is also a pre-requisite for ELEC3106: Electronics in which low level analysis and implementation of various logic gates are undertaken.

Learning outcomes

After successful completion of this course, you should be able to:

1. Analyze and design combinational circuits
2. Demonstrate a basic understanding of standard digital circuit elements such as multiplexers, decoders, etc
3. Design and optimize simple synchronous sequential circuits
4. Understand the fundamentals of the central processing unit (CPU) in a computer.
5. Demonstrate knowledge in practical aspects of digital circuits and systems, and their use in more complex systems.
6. Demonstrate understanding of the various hardware realizations of the basic digital circuit elements.
7. Demonstrate basic skills in working with computer-aided design tools, including knowing the rudiments of a hardware description language (Verilog)
8. Implement simple designs at various levels from discrete components to programmable logic devices.

This course is designed to provide the above learning outcomes which arise from targeted graduate capabilities listed in ***Appendix A***. The targeted graduate capabilities broadly support the UNSW and Faculty of Engineering graduate capabilities (listed in ***Appendix B***). This course also addresses the Engineers Australia (National Accreditation Body) Stage I competency standard as outlined in ***Appendix C***.

Syllabus

Introduction to digital systems, number systems, binary numbers, base conversion, binary codes. Binary variables, logical operators, logic gates, Boolean functions, Boolean algebra, standard forms, two-level optimization, Karnaugh maps, don’t-care conditions, multi-level optimization, high-impedance outputs. Combinational logic design procedures, technology mapping, function blocks, multi-bit variables, encoders, decoders, multiplexers, demultiplexers. Sequential circuits, basic storage elements, latches and flip-flops structures, direct inputs, finite state machines, transition equations, state tables and diagrams, state assignments, logic diagrams, Mealy and Moore models, state minimization. Arithmetic circuits, half and full adders, cascading adders, signed numbers and 2’s complements, subtractors. Programmable devices, FPGAs, hardware description languages, Verilog implementations, simulations. Introduction to computer design, datapaths, arithmetic/logic unit (ALU), shifters, instructions set. Integrated circuits (ICs), CMOS technology, CMOS logic gates.

Teaching Strategies

Delivery Mode

The teaching in this course aims at establishing a good fundamental understanding of the areas covered using:

- Formal face-to-face lectures, which provide you with a focus on the core analytical material in the course, together with qualitative, alternative explanations to aid your understanding;
- Tutorials, which allow for exercises in problem solving and allow time for you to resolve problems in understanding of lecture material;
- Laboratory sessions, which support the formal lecture material and also provide you with practical construction, measurement and debugging skills;

Learning in this course

You are expected to attend all lectures, tutorials, and labs in order to maximize learning. You must prepare well for your laboratory classes and your lab work will be assessed. In addition to the lecture notes, you should read relevant sections of the recommended text. Reading additional texts will further enhance your learning experience. Group learning is also encouraged. UNSW *assumes* that self-directed study of this kind is undertaken in addition to attending face-to-face classes throughout the course.

Lecture classes

The lectures form the core of this subject. Topics presented in lectures will generally be followed by detailed examples to provide students with the real-life applications. Detailed explanations of the topics will be available to students in the form of lecture notes and the prescribed textbook.

Tutorial classes

The tutorial problems provide students with in-depth quantitative understanding of the topics covered in lectures. Every tutorial session will have a corresponding problem sheet that covers the topics taught in the previous week. You should attempt all of your problem sheet questions in advance of attending the tutorial classes. The importance of adequate preparation prior to each tutorial cannot be overemphasized, as the effectiveness and usefulness of the tutorial depends to a large extent on this preparation. Group learning is encouraged. Answers for these questions will be discussed during the tutorial class and the tutor will cover the more complex questions in the tutorial class.

Laboratory program

The laboratory schedule is deliberately designed to provide practical, hands-on exposure to the concepts conveyed in lectures. Each week a new design problem is presented. Students will be required to step through the problem to a complete solution using the guidelines given as per lab exercise. The laboratory exercises cover a wide scope ranging from using breadboards and discrete IC components to using industry-standard design software and FPGA implementation. The exercise will follow similar (although simplified) design procedures used in industry. Students will need to bring their own breadboards previously used in ELEC1111(2) to the laboratory. Breadboards will also be offered for sale through the school office.

A broad understanding of the tools utilized in these exercises is highly encouraged and a bonus lab task will be available to students after the successful completion of all other exercises. The bonus task will carry on from the last lab exercise and will be accompanied by minimal guidelines, allowing students to further demonstrate their ability to analyse and resolve issues independently. There are two optional labs which students are encourage to carry out for an extra lab mark on the top of the bonus task. These optional labs should be done under minimal supervision and only considered or marked after the student has finished all mandatory labs.

You are required to attend laboratory from Week 4 to Week 12. Laboratory attendance WILL be kept, and you MUST attend at least 80% of labs.

The laboratory manual will be available for sale through the school office (EE & T). Every student should have the hard copy of the laboratory manual and must bring it to the laboratory class. Marks will be recorded on the laboratory manual. In addition to laboratory manual, you should also bring a lab pack. The lab pack should be collected from G15A (EE&T) prior to attending your first laboratory class. The lab pack will contain all hardware components you will need for the entire lab. Without the hardware components in the lab pack, you will not be able to do some of the laboratory activities and therefore it is important you bring you lab pack to the laboratory class. The first lab pack will be given for free. After the first one, you will be expected to pay.

Laboratory Exemption

There is no laboratory exemption for this course. Regardless of whether equivalent labs have been completed in previous courses, all students enrolled in this course for Semester 1, 2015 must take the labs. If, for medical reasons, (note that a valid medical certificate must be provided) you are unable to attend a lab, you will need to apply for a catch-up lab during another lab time, as agreed by the course convener.

Assessment

The assessment scheme in this course reflects the intention to assess your learning progress through the semester. Ongoing assessment occurs through the fortnight online quizzes, lab checkpoints (see lab manual), lab exams and two assignments.

Laboratory Assessment

The laboratory work will contribute to 15% of the overall mark. It is essential that you complete the laboratory preparation before coming to the lab. Each lab exercise will have one check point that will be marked by the lab assessors. Although there is only one check point for each lab, there are a number of results that students are required to demonstrate when marked for the check point. Therefore, students are strongly advised to: (i) record results on the lab manual; (ii) save the accomplished task or results on working directory in the lab PC; (iii) keep the working circuit on the breadboard for demonstrator to check. Demonstrators will be available to help students with any questions or difficulties.

Upon completion of a checkpoint, students will be required to write down their student and bench numbers on the Laboratory Queue Sheet and wait for the laboratory assessor to mark their work. Students may continue working on subsequent lab tasks while waiting to be assessed. Students will be required to show the working of their task for each checkpoint and answer questions asked by the assessor to demonstrate their understanding of the ideas addressed within each task.

Students will work in pair, but be marked individually. Each student will be asked a few questions. There will also be a mark for the group based on demonstrating the required lab tasks.

There will be 5% bonus marks and 2% optional lab marks available for those students who wish to attempt the additional lab task at the completion of all laboratory exercises. The exercises may require a substantial amount of time to complete successfully and students attempting it are expected to work independently as there will be minimal support provided for this task. It should be stressed, however, that marking of bonus and optional labs is subjected to the availability of demonstrators and other course staff members. Every possible effort will be made to accommodate the marking.

Laboratory Exam

There will be a laboratory exam in week 13 and it contributes 5% toward the overall mark. The exam will assess students' technical understanding of using design software tool that has been used throughout the labs in simulating, verifying, and implementing their digital circuit on the FPGA board. They will be given simple design problem, asked to implement and verify the design on the FPGA board.

Assignments

The assignments, which will consist of design challenges, form 15% of the overall mark. There will be two assignments for this subject due at the end of Week 6 and 11. The assignments will be released at the end of week 3 and week 7, respectively, on Moodle. The assignments will consist of one or more design problems and students are required to provide a complete design solution with verified implementations. All relevant workings, schematic diagrams, HDL codes, and simulations results must be attached to the submissions. Use the assignment box at the School (EE&T) office for submissions. Late submissions will attract a penalty of 10% per day (including weekends).Through these assignments, students will address most of the core topics covered in lectures thus far.

Though generic guidelines will be provided, there will be no one "correct" solution to the assignments. Students will be expected to work independently on their implementation and to be able to justify the unique design choices along the way.

Fortnight online quizzes

There will be fortnightly quizzes throughout the semester. The purpose of the quizzes is to keep students up-to-date with the lecture material and to test basic understanding of the course concepts. The fortnightly quizzes will make up 5% of the overall mark. Each quiz will consist of a number of multiple choice questions and will be marked according to the number of correct answers. The quizzes are a mandatory component of the overall assessment and failure to attempt a quiz will result in no marks being given for the quiz. Each quiz will be available for a period of two weeks and the results per quiz will be published at the end of the period. No late attempts will be permitted. **Students must attempt all quizzes to pass this subject.**

The quizzes are delivered through Moodle and will each be made available for a period of two weeks between every Saturday at 9:00am to the following Saturday at 11:59pm, after which a new quiz will become available.

Final Exam

The exam in this course is a standard closed-book 3-hour written examination, comprising five compulsory questions. It is worth 60% of the overall mark.University approved calculators are allowed. The examination tests analytical and critical thinking and general understanding of the course material in a controlled fashion. Questions may be drawn from any aspect of the course (including laboratory), unless specifically indicated otherwise by the lecturer. Marks will be assigned according to the correctness of the responses. *Please note that you must pass the final exam in order to pass the course.*

Relationship of Assessment Methods to Learning Outcomes

	Learning outcomes							
Assessment	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Laboratory practical assessments	✓	✓	✓	✓	✓	✓	✓	✓
Lab exam	✓	✓	-	-	-	-	✓	✓
Fortnight online quizzes	✓	✓	✓	✓	-	✓	✓	-
Assignment	✓	✓	✓	-	✓	-	✓	✓
Final exam	✓	✓	✓	✓	✓	✓	✓	-

Course Resources

Textbooks

Prescribed textbook

- M. M. Mano & C. R. Kime, *Logic and Computer Design Fundamentals*, 4th Edition, Prentice Hall, 2008

Reference books

- R. H. Katz & G. Borriello, *Contemporary Logic Design*, 2nd Edition, Prentice Hall, 2005,
- M. M. Mano & M. D. Ciliettl, *Digital Design*, 4th Edition, Prentice Hall, 2007.
- J. F. Wakerly, *Digital Design: Principles and Practices*, 4th Edition, Prentice Hall, 2006

On-line resources

Moodle

The course web page is hosted on the UNSW's Moodle server, which can be accessed at: https://moodle.telt.unsw.edu.au/login/index.php. All lectures, tutorial, lab and any other notes will be available on this page, as well as access to the fortnightly quizzes, student marks, discussion forums and official course announcements. It is a requirement of the course that students check this page for new announcements on a daily basis.

Mailing list

Announcements concerning course information will be given in the lectures and/or on Moodle and/or via email (which will be sent to your student email address).

Other Matters

Academic Honesty and Plagiarism

Plagiarism is the unacknowledged use of other people's work, including the copying of assignment works and laboratory results from other students. Plagiarism is considered a form of academic misconduct, and the University has very strict rules that include some severe penalties. For UNSW policies, penalties and information to help you avoid plagiarism, see http://www.lc.unsw.edu.au/plagiarism. To find out if you understand plagiarism correctly, try this short quiz: https://student.unsw.edu.au/plagiarism-quiz.

Student Responsibilities and Conduct

Students are expected to be familiar with and adhere to all UNSW policies (see https://my.unsw.edu.au/student/atoz/ABC.html), and particular attention is drawn to the following:

Workload

It is expected that you will spend at least **ten to twelve hours per week** studying a 6 UoC course, from Week 1 until the final assessment, including both face-to-face classes and *independent, self-directed study*. In periods where you need to need to complete assignments or prepare for examinations, the workload may be greater. Over-commitment has been a common source of failure for many students. You should take the required workload into account when planning how to balance study with employment and other activities.

Attendance

Regular and punctual attendance at all classes is expected. UNSW regulations state that if students attend less than 80% of scheduled classes they may be refused final assessment.

General Conduct and Behaviour

Consideration and respect for the needs of your fellow students and teaching staff is an expectation. Conduct which unduly disrupts or interferes with a class is not acceptable and students may be asked to leave the class.

Work Health and Safety

UNSW policy requires each person to work safely and responsibly, in order to avoid personal injury and to protect the safety of others.

Special Consideration and Supplementary Examinations

You must submit all assignments and attend all examinations scheduled for your course. You should seek assistance early if you suffer illness or misadventure which affects your course progress. All applications for special consideration must be **lodged online through myUNSW within 3 working days of the assessment**, not to course or school staff. For more detail, consult https://my.unsw.edu.au/student/atoz/SpecialConsideration.html.

Continual Course Improvement

This course is under constant revision in order to improve the learning outcomes for all students. Please forward any feedback (positive or negative) on the course to the course convener or via the Course and Teaching Evaluation and Improvement Process. You can also provide feedback to ELSOC who will raise your concerns at student focus group meetings.

Administrative Matters

On issues and procedures regarding such matters as special needs, equity and diversity, occupational health and safety, enrolment, rights, and general expectations of students, please refer to the School and UNSW policies:
http://www.engineering.unsw.edu.au/electrical-engineering/policies-and-procedures
https://my.unsw.edu.au/student/atoz/ABC.html

Appendix A: Targeted Graduate Capabilities

Electrical Engineering and Telecommunications programs are designed to address the following targeted capabilities which were developed by the school in conjunction with the requirements of professional and industry bodies:

- The ability to apply knowledge of basic science and fundamental technologies;
- The skills to communicate effectively, not only with engineers but also with the wider community;
- The capability to undertake challenging analysis and design problems and find optimal solutions;
- Expertise in decomposing a problem into its constituent parts, and in defining the scope of each part;
- A working knowledge of how to locate required information and use information resources to their maximum advantage;
- Proficiency in developing and implementing project plans, investigating alternative solutions, and critically evaluating differing strategies;
- An understanding of the social, cultural and global responsibilities of the professional engineer;
- The ability to work effectively as an individual or in a team;
- An understanding of professional and ethical responsibilities;
- The ability to engage in lifelong independent and reflective learning.

Appendix B: UNSW Graduate Capabilities

The course delivery methods and course content directly or indirectly addresses a number of core UNSW graduate capabilities, as follows:

- Developing scholars who have a deep understanding of their discipline, through lectures and solution of analytical problems in tutorials and assessed by assignments and written examinations.
- Developing rigorous analysis, critique, and reflection, and ability to apply knowledge and skills to solving problems. These will be achieved by the laboratory experiments and interactive checkpoint assessments and lab exams during the labs.
- Developing capable independent and collaborative enquiry, through a series of tutorials spanning the duration of the course.
- Developing digital and information literacy and lifelong learning skills through assignment work.

- Developing independent, self-directed professionals who are enterprising, innovative, creative and responsive to change, through challenging design and project tasks.

Appendix C: Engineers Australia (EA) Professional Engineer Competency Standard

	Program Intended Learning Outcomes	
PE1: Knowledge and Skill Base	PE1.1 Comprehensive, theory-based understanding of underpinning fundamentals	✓
	PE1.2 Conceptual understanding of underpinning maths, analysis, statistics, computing	✓
	PE1.3 In-depth understanding of specialist bodies of knowledge	✓
	PE1.4 Discernment of knowledge development and research directions	
	PE1.5 Knowledge of engineering design practice	✓
	PE1.6 Understanding of scope, principles, norms, accountabilities of sustainable engineering practice	
PE2: Engineering Application Ability	PE2.1 Application of established engineering methods to complex problem solving	✓
	PE2.2 Fluent application of engineering techniques, tools and resources	✓
	PE2.3 Application of systematic engineering synthesis and design processes	
	PE2.4 Application of systematic approaches to the conduct and management of engineering projects	
PE3: Professional and Personal Attributes	PE3.1 Ethical conduct and professional accountability	
	PE3.2 Effective oral and written communication (professional and lay domains)	✓
	PE3.3 Creative, innovative and pro-active demeanour	✓
	PE3.4 Professional use and management of information	✓
	PE3.5 Orderly management of self, and professional conduct	
	PE3.6 Effective team membership and team leadership	✓