

## Course Staff

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**Consultations:** You will be assigned a fixed tutor for this course during Week 1 and most of your questions should be posed and answered during the tutorials, which are scheduled in place of lectures during most weeks – see below. This is important, since your participation in tutorials contributes also to your assessment. Beyond this, the course convener will be available for consultations as much as possible during the scheduled laboratory times. If you wish to make a special consultation appointment by email or phone, the preferred time for such appointments will be Tuesday afternoons.

**Keeping Informed:** All materials for this course will be made available via <http://subjects.ee.unsw.edu.au/~elec4123>. You may also receive emails and/or announcements during the labs or the scheduled lectures or tutorials that are relevant to this course. You should read your email and visit the above-mentioned web-site regularly, since you will be deemed to be abreast of course materials and information provided therein.

## Course Summary

### Contact Hours

This course consists of a 4 hour weekly laboratory and 1 additional weekly hour of contact, which will be either a lecture or a tutorial, as detailed below. Attendance at laboratories and tutorials is mandatory, since these represent the assessed components of the course.

NB: Laboratories for this subject commence in **Week 1**

Lectures	Day	Time	Location
	Mondays W1, W4, W7 and W10	5pm-6pm	NSGlobal Theatre
<b>Tutorials</b>	Mondays W2, W3, W5, W6, W8, W9, W11 and W12	5pm-6pm	10 locations as follows: Squarehouse 205, 206, 207, 208, 211, 214, 215, 217; and Library 176A, 176B
<b>Labs</b>	Thursdays	9am-1pm	EE101/102/113/114/125

### Introduction and Aims

This is a rather unusual course, in that there are few formal lectures and there is no final or midterm examination. Instead, the course is based on weekly 4 hour laboratories, supplemented by a tutorial in 2 out of every 3 weeks. Your assessment in this subject is based largely upon these laboratories and tutorials, so you should regard attendance as compulsory and you should not seek to obtain exemption from them, except under highly unusual circumstances.

The principle purpose of this course is to test your design proficiency, through a sequence of design challenges. Some of these challenges are very basic, but there is also plenty of scope for you to demonstrate superior skills.

A secondary aim of the course is to fill in any major holes in your fundamental design knowledge, so as to ensure that all graduating students have at least a minimum level of proficiency. Although some of you might initially feel uncomfortable about this, it is important to realize that prospective employers will be very pleased indeed to know that you are able to demonstrate your proficiency. You should expect that this course will reinforce your existing knowledge and increase your confidence in design and some of the fundamental disciplines you have been studying.

A third objective of the course is to expose you to a healthy balance between team work and individual responsibility. The assessment scheme is designed to encourage you to share your ideas with your fellow students and to learn from them. At the same time, you are individually responsible for your level of proficiency. The tutorials in this course play a very important role as a forum for the exchange of ideas, where such exchange can be appropriately rewarded by the tutor.

## Course schedule

Wk	Begins	Tutorial/Lecture (Mon 5-6pm)	Laboratories (Thu 9am-1pm)
1	27 Feb	<b>Lecture: Intro and guide to Topic-1</b>	Topic-1: Electronic Circuits
2	6 Mar	Tut: Electronic Circuits	Topic-1: Electronic Circuits
3	13 Mar	Tut: Electronic Circuits	Topic-1: Electronic Circuits
4	20 Mar	<b>Lecture: Post-mortem and guide to Topic-2</b>	Topic-2: Signal Processing
5	27 Mar	Tut: Signal Processing	Topic-2: Signal Processing
6	3 Apr	Tut: Signal Processing	Topic-2: Signal Processing
7	10 Apr	<b>Lecture: Post-mortem + guide to Topic-3</b>	Topic-3: Control Systems
Mid Session Recess			
8	24 Apr	Tut: Control Systems	Topic-3: Control Systems
9	1 May	Tut: Control Systems	Topic-3: Control Systems
10	8 May	<b>Lecture: Post-mortem + guide to Electives</b>	Elective Topic: no assessment
11	15 May	Tut: Elective	Elective Topic: no assessment
12	22 May	Tut: Elective	Elective Topic: <b>assessment</b>
13	29 May	<b>no tut or lecture</b>	<b>Group report due by 5pm Thursday</b>

## Assessment

The marks for this course will be assigned as follows:

Assessment Component	Basis	Marks
Contribution within tutorials	individual	20%
Achievement of design objectives, as demonstrated in labs	individual (T1-T2) group (T3-T4)	40% (4x10%)
Understanding of relevant subject material, as demonstrated in labs	individual	28% (4x7%)
Group report on elective topic	group	12%

## Course Details

### Credits

This is a 6 UoC course and the expected average workload is 10–12 hours per week throughout the semester. Note, however, that since this course has no final examination,

the workload of the course is compacted into just 12 weeks, so you should adjust your effort accordingly.

### Relationship to Other Courses

This is a 4<sup>th</sup> year course in the School of Electrical Engineering and Telecommunications, which is a core component of the BE programs (Electrical and Telecommunications) offered by the School.

This course directly ties into core courses in Electronics, Signal Processing, Control, Telecommunications, Data Networks and Energy Systems which you should have already taken (typically in the third year of your program). See below for more on what is expected.

### Pre-requisites and Assumed Knowledge

The course has three core topics, for which the following knowledge is assumed:

- Electronics (to the level of ELEC3016)
- Signal Processing (to the level of ELEC3104)
- Control Systems (to the level of ELEC3114).

Through these and other courses, it is assumed that students have also developed good computer literacy and familiarity with Matlab, which is used in some topics.

### Learning outcomes

Upon successful completion of this course, the student should:

1. Have demonstrated an ability to work both individually and within a group, to produce designs which draw upon a number of disciplines previously studied in other courses.
  - *The 4 design topics and 12 laboratory sessions all reinforce and assess these abilities.*
2. Have demonstrated an ability to contribute to and learn from peers.
  - *The elective design topic and the tutorial sessions all reinforce and assess this ability.*
3. Have demonstrated a sufficient level of understanding and skill within a range of disciplines, together with an ability to explain design decisions.
  - *The assessment methodology in laboratories deliberately reinforce and assess these outcomes.*

This course is designed to provide the above learning outcomes which arise from targeted graduate capabilities listed in **Appendix A**. The targeted graduate capabilities broadly support the UNSW and Faculty of Engineering graduate capabilities (listed in **Appendix B**). This course also addresses the Engineers Australia (National Accreditation Body) Stage I competency standard as outlined in **Appendix C**.

### Syllabus

The course involves four competency components, as follows:

- Electronic Circuit Design: Devices, amplifiers, tuned circuits, opamp circuits, etc.
- Control System Design: Feedback and stability, linear control, non-linear control, data acquisition and sampling, etc.
- Signal Processing Design: Filter design, frequency response, spectrum analysis, BIBO analysis, etc.
- Power System Design: Transformer, motor, power electronic converter, power factor, harmonics, etc.

Laboratory assessment requires the design, construction and understanding of working solutions to specified problems.

## **Teaching Strategies**

The teaching in this subject is heavily focused on laboratories. Each of 4 design topics has 3 assigned laboratories, each 4 hours in duration. The laboratories are designed to develop and assess proficiency. The majority of the assessment is individual, with a focus on objectively working solutions, in addition to understanding.

The laboratories are complemented by a series of tutorials, which provide an opportunity for reflection, learning and peer support. Since each design topic lasts for 3 weeks, the associated two tutorials allow you to ask questions, to get helpful advice from your peers as well as the tutor, and to reflect consciously and productively on the difficulties you and your peers may have encountered, along with ways to overcome these difficulties.

For each design topic, the weekly iteration between laboratories and tutorials forms a learning cycle, which has the potential to be very effective. A lecture every 3 weeks serves to initiate each cycle and also to provide a final reflection on the previous cycle.

Through these mechanisms, the course aims to build and ensure proficiency in the core areas of your program of study.

## **Design Topics**

The course is divided into a sequence of three “core design topics” and one “elective design topic,” each of which is assigned 3 weeks in the laboratory timetable. The core design topics are: 1) Electronic Circuits; 2) Signal Processing; and 3) Control Systems. The elective topics are: 4a) Telecommunications; 4b) Data Networks; and 4c) Energy Systems.

Each of the core topics consists of a sequence of design tasks, with progressively higher complexity. Design tasks for the core topics must be completed individually, although you are encouraged to discuss the topics with your fellow students. The third design topic (Control Systems) may prove an exception to this rule, where students will need to work more tightly in pairs due to equipment limitations.

The elective design is performed in groups of at most 4 students; you must organize yourself into such a group and nominate which of the elective topics you intend to pursue by the end of Week 7. You will be provided with further instructions on how to do this. Unlike the first three design topics, the elective design is assessed only in the final week.

## **Individual Learning**

Preparation for labs is essential to success in this course. You will find yourself revising material from previous courses, discussing problems with your peers, seeking help from your tutorial group, and struggling to find and solve problems you encounter with your design or implementation in the laboratory. All of these are outstanding learning opportunities.

## **Group Learning**

Tutorials provide a group learning experience. The first tutorial for a design topic follows the first laboratory session for that topic, so all students should have attempted and hopefully completed some of the design tasks. In general, some students will make progress faster than others, putting them in a good position to advise students who have encountered more difficulties. This type of interaction represents a good learning experience for all parties, and forms the foundation of the tutorial sessions.

The elective design topic is a team effort, having larger scope and less incremental objectives than the first three design topics. To succeed in this topic, you will need to work effectively as a team member or leader. Moreover, each group is required to submit a report

(due in Week 13) describing the design principles, implementation, outcomes and final reflections. The report itself will need to be a group effort.

### **Laboratory Exemption**

There is no laboratory exemption for this course. If, for medical reasons, (note that a valid medical certificate must be provided) you are unable to be assessed for your laboratory work, you will need to **seek permission from the course convener** to be assessed in a subsequent week.

## **Assessment**

### **Assessment of core design tasks**

All completed tasks for the three core design topics are to be assessed during the laboratory sessions by one of the laboratory demonstrators. Once you have completed a task, you should add your name to a list maintained by the demonstrators in your laboratory, so that you can be assessed as quickly as possible. You cannot expect to be assessed for all of the tasks you have completed during the final laboratory session of the topic, since this can place an unacceptable burden on the demonstrators' time.

Of the 17% of the overall course assessment that is associated with each core design topic, 10% is awarded based on actual outcomes. You cannot expect to obtain any of these marks for a solution which does not actually work or achieve the task objectives to some extent. The remaining 7% is awarded for your understanding of the design problem and your own design.

Assessment is individual. Except where otherwise indicated, you may not present a group design or implementation for assessment within the core design topics.

### **Assessment for the elective design topic**

The elective design topic is a group activity, for which all assessment will take place in Week 12. Of the 17% of the overall course assessment that is associated with this topic (excluding the report), 10% is again awarded based on actual outcomes, while the remaining 7% is awarded based on individual understanding of the design problem and the group's solution. Individual group members will be separately interviewed to establish this second component. Except where a group member has made a clearly disproportionate contribution to the project, the performance component of the mark will be awarded equally to all students in the group.

### **Assessment for tutorial participation and contribution**

Your tutor will keep track of students who contribute to the tutorial, assigning a final mark that reflects this contribution over the course of the session. This mark will form 20% of your overall assessment for the course. Commendable contributions in tutorials include the following:

1. Sharing solutions to problems faced by other students in the tutorial.
2. Sharing difficulties or concerns with the rest of the group, in a way that demonstrates thought and preparation.
3. Contributing to the understanding of the design problem itself.

During the two tutorials that are concerned with the elective design topic, there will typically be several different design challenges being tackled by groups within the same tutorial. These tutorials provide an opportunity for students working on different design challenges to share ideas that help each other. The ability and willingness to do this are important attributes of a professional engineer.

## Relationship of Assessment Methods to Learning Outcomes

Assessment	Learning outcomes		
	1	2	3
Core design tasks	✓	-	✓
Elective design topic	✓	✓	✓
Elective design group report	✓	✓	✓
Tutorial contribution	✓	✓	✓

## Course Resources

### Textbooks

There are no specific texts for this course, but you should consider your lecture notes and text books from earlier classes in Electronics, Signal Processing, Control, Telecommunications, Data Networks and/or Energy Systems to be useful resources.

### On-line resources

Design tasks and other materials for this course will be made available via the course web-page at <http://subjects.ee.unsw.edu.au/~elec4123>.

### Mailing list

Announcements concerning course information will be made via the course web-page, in lectures, tutorials, laboratories and/or via email. You should note that any course related email will be sent exclusively to your UNSW student email address.

## Other Matters

### Academic Honesty and Plagiarism

Plagiarism is the unacknowledged use of other people's work, including the copying of assignment works and laboratory results from other students. Plagiarism is considered a form of academic misconduct, and the University has very strict rules that include some severe penalties. For UNSW policies, penalties and information to help you avoid plagiarism, see <https://student.unsw.edu.au/plagiarism>. To find out if you understand plagiarism correctly, try this short quiz: <https://student.unsw.edu.au/plagiarism-quiz>.

### Student Responsibilities and Conduct

Students are expected to be familiar with and adhere to all UNSW policies (see <https://student.unsw.edu.au/guide>), and particular attention is drawn to the following:

### Workload

It is expected that you will spend at least **ten to twelve hours per week** studying a 6 UoC course, from Week 1 until the final assessment, including both face-to-face classes and *independent, self-directed study*. Since this course has no final examination, you should plan to spend more time during the session itself. You should take the required workload into account when planning how to balance study with employment and other activities.

### Attendance

Regular and punctual attendance at all classes is expected. UNSW regulations state that if students attend less than 80% of scheduled classes they may be refused final assessment.

## General Conduct and Behaviour

Consideration and respect for the needs of your fellow students and teaching staff is an expectation. Conduct which unduly disrupts or interferes with a class is not acceptable and students may be asked to leave the class.

## Work Health and Safety

UNSW policy requires each person to work safely and responsibly, in order to avoid personal injury and to protect the safety of others.

## Special Consideration and Supplementary Assessment

Each laboratory session is an opportunity for assessment in this course. You are expected to attend all laboratory sessions. Special consideration will be shown to students suffering from illness or misadventure, which can generally be accommodated with the 3 weekly cycle associated with each proficiency topic. You should seek assistance early if you suffer illness or misadventure which affects your progress with the design topics or ability to be assessed, especially where this interferes with your ability to be assessed by the final week of each proficiency topic. All applications for special consideration must be **lodged online through myUNSW within 3 working days of the affected assessment**, not to course or school staff. For more detail, consult <https://student.unsw.edu.au/special-consideration>.

## Continual Course Improvement

This course is under constant revision in order to improve the learning outcomes for all students. Please forward any feedback (positive or negative) on the course to the course convener or via the “myExperience” process. You can also provide feedback to ELSOC who will raise your concerns at student focus group meetings.

## Administrative Matters

On issues and procedures regarding such matters as special needs, equity and diversity, occupational health and safety, enrolment, rights, and general expectations of students, please refer to the School and UNSW policies:

<https://student.unsw.edu.au/guide>

<https://www.engineering.unsw.edu.au/electrical-engineering/resources>

## Appendix A: Targeted Graduate Capabilities

Electrical Engineering and Telecommunications programs are designed to address the following targeted capabilities which were developed by the school in conjunction with the requirements of professional and industry bodies:

- The ability to apply knowledge of basic science and fundamental technologies;
- The skills to communicate effectively, not only with engineers but also with the wider community;
- The capability to undertake challenging analysis and design problems and find optimal solutions;
- Expertise in decomposing a problem into its constituent parts, and in defining the scope of each part;
- A working knowledge of how to locate required information and use information resources to their maximum advantage;

- Proficiency in developing and implementing project plans, investigating alternative solutions, and critically evaluating differing strategies;
- An understanding of the social, cultural and global responsibilities of the professional engineer;
- The ability to work effectively as an individual or in a team;
- An understanding of professional and ethical responsibilities;
- The ability to engage in lifelong independent and reflective learning.

## Appendix B: UNSW Graduate Capabilities

The course delivery methods and course content directly or indirectly addresses a number of core UNSW graduate capabilities, as follows:

- Developing rigorous analysis, critique, and reflection, and ability to apply knowledge and skills to solving problems. These will be achieved through the laboratory program and the associated design tasks, as assessed in the lab.
- Developing ethical practitioners who are collaborative and effective team workers, through group activities and tutorials.
- Developing independent, self-directed professionals who are enterprising, innovative, creative and responsive to change, through challenging design and project tasks.

## Appendix C: Engineers Australia (EA) Professional Engineer Competency Standard

	Program Intended Learning Outcomes	
PE1: Knowledge and Skill Base	PE1.1 Comprehensive, theory-based understanding of underpinning fundamentals	
	PE1.2 Conceptual understanding of underpinning maths, analysis, statistics, computing	
	PE1.3 In-depth understanding of specialist bodies of knowledge	✓
	PE1.4 Discernment of knowledge development and research directions	
	PE1.5 Knowledge of engineering design practice	✓
	PE1.6 Understanding of scope, principles, norms, accountabilities of sustainable engineering practice	
PE2: Engineering Application Ability	PE2.1 Application of established engineering methods to complex problem solving	✓
	PE2.2 Fluent application of engineering techniques, tools and resources	✓
	PE2.3 Application of systematic engineering synthesis and design processes	✓
	PE2.4 Application of systematic approaches to the conduct and management of engineering projects	✓
a n d P e	PE3.1 Ethical conduct and professional accountability	



	PE3.2 Effective oral and written communication (professional and lay domains)	✓
	PE3.3 Creative, innovative and pro-active demeanour	
	PE3.4 Professional use and management of information	
	PE3.5 Orderly management of self, and professional conduct	
	PE3.6 Effective team membership and team leadership	✓