School of Electrical Engineering and Telecommunications

Term 2, 2019
Course Outline

ELEC9704
VLSI Technology

COURSE STAFF

Course Conveners: Prof. Chee Yee KWOK, Room 344
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Consultations: You are encouraged to ask questions on the course material, after the lecture class times in the first instance, rather than via email. Lecturer consultation times will be advised during lectures. You are welcome to email the tutor or laboratory demonstrator, who can answer your questions on this course and can also provide you with consultation times. ALL email enquiries should be made from your student email address with ELEC9704 in the subject line; otherwise they will not be answered.

Keeping Informed: Announcements may be made during classes, via email (to your student email address) and/or via online learning and teaching platforms – in this course, we will use Moodle https://moodle.telt.unsw.edu.au/login/index.php. Please note that you will be deemed to have received this information, so you should take careful note of all announcements.

COURSE SUMMARY

This is a postgraduate course. The main focus of the subject is on semiconductor processes involved in the fabrication of very very large scale silicon integrated circuits with billions of transistors. Initially, the course will attempt to study a comprehensive range of individual processes, and towards the end, these processes are integrated together into a process schedule for the fabrication of CMOS and bipolar VLSI circuits. Because integrated circuits fail from time to time, failure analysis plays an important role in process development. The course will include lectures on analytical techniques employed in understanding the causes of failure in order to modify the processes for better reliability.

VLSI technology is moving at a very rapid pace, spurred by the demand for further and further miniaturisation, greater circuit complexity and functionality per chip. Minimum feature sizes in production in '60s were tens of μm. In the '70s, it was several μm, in the '80s it was about 1μm, in the '90s it is submicron and now in the 21st century, it is the deep-deep-sub micron (<10nm range). Acronyms have evolved from SSI to MSI to LSI to VLSI to ULSI to GSI and now Terascale. In the past 20 years, 'ultimate' limits of scaling were predicted, and only to be surpassed years later. Wafer size of 300mm is now in production and has moved to 450mm!!

The subject will enable students to have a broad grasp of the multi-disciplinary nature of VLSI technology, bringing together the know-how of physicist, chemist, engineers and mathematicians. It will provide the fundamental knowledge for students, who want to enter the semiconductor industry. It is an exciting field of research and we should count ourselves fortunate to be witnessing and participating in this era of unparalleled 'technology explosion'.

Contact Hours

This postgraduate course consists of 3 hours of lectures in the evenings. Problem discussions are included in the lectures and will not be treated as separate tutorials. **Special note: for the first 4 weeks, the lectures will be 3 hrs per week, for weeks 5-10 the lectures will be 4 hours per weeks**

Lectures	Day	Time	Location
Weeks 1-4	Tuesday	6 – 9pm	CLB 3
Weeks 5-10	Tuesday	5 -- 9pm	CLB 3

Context and Aims

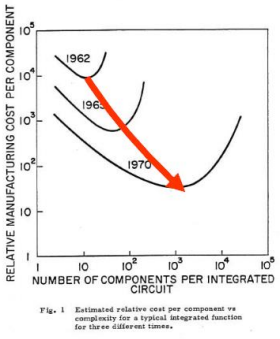
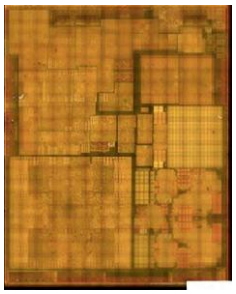


Fig. 1 Estimated relative cost per component vs complexity for a typical integrated function for three different times.

"Reduced cost is one of the big attractions of integrated electronics, and the cost advantage continues to increase as the technology evolves toward the production of larger and larger circuit functions on a single semiconductor substrate"

Electronics, Volume 38, No. 8, April 19, 1965



"The Apple A8 is, of course, the most interesting element in the new iPhone 6. All clues point to it being manufactured by TSMC on a 20nm node, and that makes it one of the first 20nm chips out there. The A8 is also some 13% smaller than last year's A7, while packing nearly double the amount of transistors – up from around 1 billion to some 2 billion transistors in the Apple A8. And yes, RAM is still 1GB on the iPhone". *ITRS 2015 Paolo Report*

The above examples give us an amazing snapshot of how far the technology has moved over the last 50 years. The iPhone 6 is still fresh in our minds. All these would not have been possible if it were not for the advances in scaling of devices from tens of microns to tens of nanometers in today's technology. How is this possible? That is the subject of this course.

Aims:

The course aims to familiarize students with silicon integrated technology and equip them with fundamental know-hows on which they build their future career in the semiconductor fabrication foundries and research areas.

Indicative Lecture Schedule

Period	Hrs	Lecture Topics	Due dates
Week 1 (4/6)	6-9 pm	Introduction to VLSI Technology: historical perspective and trends today. Silicon crystal growth.	
Week 2 (11/6)	6-9 pm	Wafer preparation. Oxidation of silicon (1)	
Week 3 (18/6)	6-9 pm	Oxidation of silicon (2) & Impurity diffusion in silicon	
Week 4 (25/6)	6-9 pm	Ion implantation & Epitaxial growth	Assignment 1 release
Week 5 (2/7)	5-9 pm	Thin Film deposition techniques. Wet etching.	
Week 6 (9/7)	5-9 pm	Dry etching. Lithography	Assignment 1 due 9/7/2019
Week 7 (16/7)	5-9 pm	Lithography, Metallisation	Mid-term exam
Week 8 (23/7)	5-9 pm	VLSI process integration, 3D integration, FINFETs	Assignment 2 release
Week 9 (30/7)	5-9 pm	VLSI process integration, 3D integration, FINFETs. Failure Analysis (1)	
Week 10 (6/8)	5-9 pm	Failure Analysis Techniques (2) & revision	Assignment 2 due 6/8/2019

Assessment

Assignment 1	**12.5%**
Assignment 2	**12.5%**
Mid-Term Exam	**20%**
Final Exam (2 hours)	**55%**

Course Details

Credits

This is a 6 UoC course and the expected workload is 10 hours per week throughout the 10 weeks term.

Relationship to Other Courses

This is a postgraduate course offered to students in the Master of Engineering Science at the University of New South Wales. The course complements the Microelectronics Design course ELEC4602 and Mixed Signal Design course ELEC 9701. It lays the ground work for Microsystems Course ELEC 9703.

Pre-requisites and Assumed Knowledge
There is no specific pre-requisite for the course. However, it suits students who are familiar with semiconductor device and microelectronics design, similar to the courses covered in ELEC4603 and ELEC4602 in the UNSW EE undergraduate program. It is further assumed that the students are familiar with some basic chemistry. The course is multidisciplinary in nature.

Learning outcomes
After the successful completion of the course, the student will be able to:

1. Develop an appreciation of the technology trends
2. Understand the basic process steps in making integrated circuits
3. Understand the technology limitations of each process
4. Understand the impact of these limitations on the IC designer's options
5. Understand how these steps are integrated in the process to make integrated circuits

This course is designed to provide the above learning outcomes which arise from targeted graduate capabilities listed in ***Appendix A***. The targeted graduate capabilities broadly support the UNSW and Faculty of Engineering graduate capabilities (listed in ***Appendix B***). This course also addresses the Engineers Australia (National Accreditation Body) Stage I competency standard as outlined in ***Appendix C***.

Syllabus
Introduction to VLSI Technology: historical perspective and trends today; Silicon crystal growth and wafer preparation; Oxidation of silicon; Impurity diffusion in silicon; Ion implantation of impurities into silicon; Epitaxy growth on silicon substrates; Thin Film deposition techniques; Wet etching, Dry(plasma) etching; Lithography, Metallization; VLSI process integration; 3D integration; Failure Analysis Techniques.

Teaching Strategies

Delivery Mode
The teaching in this course aims at establishing a good fundamental understanding of the areas covered using:

- Formal face-to-face lectures, which provide you with a focus on the core analytical material in the course, together with qualitative, alternative explanations to aid your understanding;
- There are no separate tutorials but done in lectures from time to time.
- Where possible, lectures will be videoed and uploaded to moodle for students to clarify specific aspects of the lecture. It is not a substitute for missed lectures.

Learning in this course
You are expected to attend <u>all</u> lectures, and attempt assignments in order to maximise learning. In addition to the lecture notes/recorded lecture videos, you should read relevant sections of the recommended reference text. Reading additional texts will further enhance your learning experience. Group learning is also encouraged. UNSW *assumes* that self-directed study of this kind is undertaken in addition to attending face-to-face classes throughout the course.

Tutorial classes
There are no separate tutorial classes but problems will be dealt with in class.

Laboratory program
There are no laboratory programs. However, a short lab tour of Australian National Fabrication Facility (NSW node) is arranged towards the later part of the course.

Assessment

Assignment 1	12.5%
Assignment 2	12.5%
Mid-term exam (**closed book**)	20%
Final Exam (2 hours **closed book**)	55%

1. ***Assignments:*** There are two compulsory written **assignments** for this course, which will be released on the course Moodle after Weeks 4 and 8 respectively. The assignments will each be worth 12.5% of the overall mark in total for this course. It is expected that the students complete assignments on their own. Assignment submissions dates are set on Tuesdays of week 6 and 10 for each assignment respectively.

2. ***Mid-Term exam:*** A mid-term will be conducted on Tuesday of week 7. Exact time of the exam will be announced during the course. It may be conducted outside of the normal class lecture times of 6-9pm. It will be a closed book exam.

3. ***Final exam***: It will be a closed book 2 hour final exam.

The assessment scheme in this course reflects the intention to assess your learning progress through the term.

Mid-Term and Final Exams
The exams in this course are **CLOSED-BOOK** written examination. University approved calculators are allowed. The examination tests analytical and critical thinking and general understanding of the course material in a controlled fashion. Questions may be drawn from any aspect of the course, unless specifically indicated otherwise by the lecturer. Sections of the course examined in the mid-session exam will not be examined again in the final exam. Further details will be given in the lectures. Marks will be assigned according to the correctness of the answers and not the volume of written material in the answer scripts.

Relationship of Assessment Methods to Learning Outcomes

	Learning outcomes							
Assessment	**1**	**2**	**3**	**4**	**5**			
Assignment1	x	x	x	x				
Assignment 2	x	x	x	x				
Mid-session exam	x	x	x	x	x			
Final exam	x	x	x	x	x			

COURSE RESOURCES

Textbooks

Because of the breadth of the course, no textbook is set for this course but a good reference book to buy is by JD Plummer or S Sze. The following are the recommended reference books.

1. JD Plummer, MD Deal, PB Griffin, “Silicon VLSI Technology”, Prentice Hall, 2000.
2. S K Ghandi, “VLSI Fabrication Principles”, Wiley.
3. S M Sze, “VLSI Technology”, McGraw-Hill.
4. S A Campbell, “The science and Engineering of Microelectronic Fabrication”, Oxford University Press.
5. R A Levy, “Microelectronic Materials and Processes”, Kluwer.
6. E H Nicollian and J R Brews, “MOS Physics and Technology”, Wiley.
7. D K Schroder, “Semiconductor material and device characterisation”, Wiley Interscience

OTHER MATTERS

Dates to note

Important Dates available at: https://student.unsw.edu.au/dates

Academic Honesty and Plagiarism

Plagiarism is the unacknowledged use of other people’s work, including the copying of assignment works and laboratory results from other students. Plagiarism is considered a form of academic misconduct, and the University has very strict rules that include some severe penalties. For UNSW policies, penalties and information to help you avoid plagiarism, see https://student.unsw.edu.au/plagiarism. To find out if you understand plagiarism correctly, try this short quiz: https://student.unsw.edu.au/plagiarism-quiz.

Student Responsibilities and Conduct

Students are expected to be familiar with and adhere to all UNSW policies (see https://student.unsw.edu.au/guide), and particular attention is drawn to the following:

Workload

It is expected that you will spend at least **ten to twelve hours per week** studying a 6 UoC course, from Week 1 until the final assessment, including both face-to-face classes and *independent, self-directed study*. In periods where you need to need to complete assignments or prepare for examinations, the workload may be greater. Over-commitment has been a common source of failure for many students. You should take the required workload into account when planning how to balance study with employment and other activities.

Attendance

Regular and punctual attendance at all classes is expected. UNSW regulations state that if students attend less than 80% of scheduled classes they may be refused final assessment.

General Conduct and Behaviour

Consideration and respect for the needs of your fellow students and teaching staff is an expectation. Conduct which unduly disrupts or interferes with a class is not acceptable and students may be asked to leave the class.

Work Health and Safety

UNSW policy requires each person to work safely and responsibly, in order to avoid personal injury and to protect the safety of others.

Special Consideration and Supplementary Examinations

You must submit all assignments and attend all examinations scheduled for your course. As of Term 1 2019, assessment of applications for Special Consideration (https://student.unsw.edu.au/special-consideration) will be managed centrally and the University has introduced a “fit to sit/submit” rule. You will no longer be required to take your original documentation to The Nucleus for verification. Instead, UNSW will conduct source checks on documentation for verification purposes. You can apply for

special consideration when illness or other circumstances beyond your control interfere with an assessment performance. If you need to submit an application for special consideration for an exam or assessment, you must submit the application **prior to the start** of the exam or before the assessment is submitted, except where illness or misadventure prevent you from doing so. If you sit an exam or submit an assignment, you are declaring yourself well enough to do so.

Continual Course Improvement

This course is under constant revision in order to improve the learning outcomes for all students. Please forward any feedback (positive or negative) on the course to the course convener or via the online student survey myExperience. You can also provide feedback to ELSOC who will raise your concerns at the student focus group meetings. As a result of previous feedback obtained for this course and in our efforts to provide a rich and meaningful learning experience, we have continued to evaluate and modify our delivery and assessment methods.

Administrative Matters

On issues and procedures regarding such matters as special needs, equity and diversity, occupational health and safety, enrolment, rights, and general expectations of students, please refer to the School and UNSW policies:

https://student.unsw.edu.au/guide

https://www.engineering.unsw.edu.au/electrical-engineering/resources

APPENDICES

Appendix A: Targeted Graduate Capabilities

Electrical Engineering and Telecommunications programs are designed to address the following targeted capabilities which were developed by the school in conjunction with the requirements of professional and industry bodies:

- The ability to apply knowledge of basic science and fundamental technologies;
- The skills to communicate effectively, not only with engineers but also with the wider community;
- The capability to undertake challenging analysis and design problems and find optimal solutions;
- Expertise in decomposing a problem into its constituent parts, and in defining the scope of each part;
- A working knowledge of how to locate required information and use information resources to their maximum advantage;
- Proficiency in developing and implementing project plans, investigating alternative solutions, and critically evaluating differing strategies;
- An understanding of the social, cultural and global responsibilities of the professional engineer;
- The ability to work effectively as an individual or in a team;
- An understanding of professional and ethical responsibilities;
- The ability to engage in lifelong independent and reflective learning.

Appendix B: UNSW Graduate Capabilities

The course delivery methods and course content directly or indirectly addresses a number of core UNSW graduate capabilities, as follows

- Developing scholars who have a deep understanding of their discipline, through lectures and solution of analytical problems in tutorials and assessed by assignments and written examinations.
- Developing rigorous analysis, critique, and reflection, and ability to apply knowledge and skills to solving problems. These will be achieved by the laboratory experiments and interactive checkpoint assessments and lab exams during the labs.
- Developing capable independent and collaborative enquiry, through a series of assignments spanning the duration of the course.

- Developing digital and information literacy and lifelong learning skills through assignment work.
- Developing ethical practitioners who are collaborative and effective team workers, through group activities, seminars and tutorials.
- Developing independent, self-directed professionals who are enterprising, innovative, creative and responsive to change, through challenging design and project tasks.

Appendix C: Engineers Australia (EA) Professional Engineer Competency Standard

	Program Intended Learning Outcomes	
PE1: Knowledge and Skill Base	PE1.1 Comprehensive, theory-based understanding of underpinning fundamentals	✓
	PE1.2 Conceptual understanding of underpinning maths, analysis, statistics, computing	✓
	PE1.3 In-depth understanding of specialist bodies of knowledge	✓
	PE1.4 Discernment of knowledge development and research directions	
	PE1.5 Knowledge of engineering design practice	✓
	PE1.6 Understanding of scope, principles, norms, accountabilities of sustainable engineering practice	
PE2: Engineering Application Ability	PE2.1 Application of established engineering methods to complex problem solving	✓
	PE2.2 Fluent application of engineering techniques, tools and resources	✓
	PE2.3 Application of systematic engineering synthesis and design processes	
	PE2.4 Application of systematic approaches to the conduct and management of engineering projects	
PE3: Professional and Personal Attributes	PE3.1 Ethical conduct and professional accountability	
	PE3.2 Effective oral and written communication (professional and lay domains)	✓
	PE3.3 Creative, innovative and pro-active demeanour	✓
	PE3.4 Professional use and management of information	✓
	PE3.5 Orderly management of self, and professional conduct	
	PE3.6 Effective team membership and team leadership	✓