COURSE SUMMARY

Contact Hours

This course involves

- **Two 3-hour** of scheduled laboratory contacts per week (total 6 hours per week)
- **Two open labs per week** (two 9-hour sessions per week, but you can only book total two 4.5-hour sessions of open lab per week. The last open lab every fortnight is catch-up lab)
- **One-hour introductory lecture in Week 1** (there will no other lectures) as detailed on the next page.

Attendance at laboratories is mandatory, since these are the primary assessed components of the course. All laboratories are assessment opportunities.

Attending open labs is optional. Attending catch-up labs is buy the approval of the course coordinator. More details on open labs and catch-up labs are provided in TEACHING STRATEGIES and ASSESSMENT sections.

Please note that there are no tutorials for this course and please ignore the timetabling.
<table>
<thead>
<tr>
<th>Session</th>
<th>Day</th>
<th>Time</th>
<th>Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lecture: W1 only</td>
<td>Monday</td>
<td>4pm – 5pm</td>
<td>Central Lecture Block (K-E19-103) [Click here for the map]</td>
</tr>
<tr>
<td>Scheduled Laboratories*: W1 – W4, W6 – W8, W10, W11</td>
<td>Monday</td>
<td>5pm – 8pm</td>
<td>Labs 201, 224, 225, and 214 in EE&amp;T Building (G17)</td>
</tr>
<tr>
<td></td>
<td>Wednesday</td>
<td>3pm – 6pm</td>
<td></td>
</tr>
<tr>
<td>Open labs and catch-up labs**: W1 – W4, W6 – W8, W10, W11</td>
<td>Tuesday</td>
<td>11am – 8pm</td>
<td>Lab 201 in EE&amp;T Building (G17)</td>
</tr>
<tr>
<td></td>
<td>Friday</td>
<td>10am – 7pm</td>
<td></td>
</tr>
</tbody>
</table>

* There will be no scheduled labs in Week 5 and Week 9. Week 11 is the makeup lab for a public holiday on Mon of Week 9, which will be the final assessment of the last topic of the course.
** Open labs and catch-up labs are not shown in the official timetabling, but you need to include them in your calendar. Also, every fortnight, the Friday session is reserved for catch-up lab for the corresponding topic on that week.

**Context and Aims**

This is a rather unusual course, in that there is no final or mid-term examination and most of your contact hours are spent in the laboratory. The course is organized around 4 proficiency topics, each of which has four formal lab sessions each lasting 3 hours, plus two open labs, and a catch-up lab included in the course schedule. The first three topics cover the core disciplines of Electronics, Signal Processing and Control Systems, while the fourth topic involves an elective choice of two or three different projects. With some exceptions for the elective topic, all formal lab sessions are assessment opportunities. To accommodate the 10-week term, a new schedule has been devised to incorporate open labs and catch-up lab into the course schedule.

The first 15min of each Mon lab session will be dedicated to keep the course on track and to help to correct weaknesses in your understanding. This is a replacement of the 1-hour Lectures in the previous offerings of the course. We will use the video conferencing feature of the EE&T labs so that all students can tune in to the interactive presentations while being in different rooms.

The principle purpose of this course is to test your design proficiency, through a sequence of design challenges. Some of the challenges are very basic, but there is also plenty of scope for you to demonstrate superior skills. The design challenges within each of the core (non-elective) topics are organized into 4 or 5 tasks that can be undertaken and assessed progressively. Your designs, implementation and assessment for the core topics are to be undertaken on an individual basis, not as group work. Moreover, you are expected to regard the laboratory sessions as miniature examinations.

A secondary aim of the course is to fill in any major holes in your fundamental design knowledge, to ensure that all graduating students have at least a minimum level of proficiency. Although some of you might initially feel uncomfortable about this, it is important to realise that prospective employers will be very pleased indeed to know that you are able to demonstrate your proficiency. You should expect that this course will reinforce your existing knowledge and increase your confidence in design and some of the fundamental disciplines you have been studying. Opportunities to correct misunderstandings mostly occur between laboratory sessions, including within the course lectures.

A third objective of the course is to expose you to a healthy balance between teamwork and individual responsibility. For practical reasons, team-based design is restricted to the elective topic, which takes place over Weeks 8-10 and is assessed differently from the other topics. You will be assigned a tutor who can both help to keep you on track and also keep an eye on the functioning of your team and the level of contribution that each team member appears to be making to the design. The elective topic will involve both individual and group assessment components.
## Indicative Laboratory Schedule

<table>
<thead>
<tr>
<th>Period</th>
<th>Summary of Laboratory Program</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Monday (5pm-8pm)</td>
</tr>
<tr>
<td>Week 1</td>
<td>Topic 1: Electronics</td>
</tr>
<tr>
<td>Week 2</td>
<td>Topic 1: Electronics</td>
</tr>
<tr>
<td>Week 3</td>
<td>Topic 2: Signal Processing</td>
</tr>
<tr>
<td>Week 4</td>
<td>Topic 2: Signal Processing</td>
</tr>
<tr>
<td>Week 5</td>
<td>No scheduled lab</td>
</tr>
<tr>
<td>Week 6</td>
<td>Topic 3: Control Systems</td>
</tr>
<tr>
<td>Week 7</td>
<td>Topic 3: Control Systems</td>
</tr>
<tr>
<td>Week 8</td>
<td>Topic 4: Elective</td>
</tr>
<tr>
<td>Week 9</td>
<td>Public Holiday</td>
</tr>
<tr>
<td>Week 10</td>
<td>Topic 4: Elective</td>
</tr>
<tr>
<td>Week 11</td>
<td>Topic 4: Elective (Final assessment)</td>
</tr>
<tr>
<td>Week 12</td>
<td></td>
</tr>
</tbody>
</table>

## Assessment

The total mark of each core topic is 24% and the elective topic is worth 28% (four/4 topics in total 100%). The marks breakdown for each aspect of the topics for this course will be assigned as follows:

<table>
<thead>
<tr>
<th>Assessment Concept</th>
<th>Basis</th>
<th>Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core Topics: Achievement of design objectives, as demonstrated in labs</td>
<td>Individual</td>
<td>36% (3×12%)</td>
</tr>
<tr>
<td>Core Topics: Understanding of relevant subject material, as demonstrated in labs</td>
<td>Individual</td>
<td>30% (3×10%)</td>
</tr>
<tr>
<td>Core Topics: Reflective task, submitted online, core topics T1-T3</td>
<td>Individual</td>
<td>6% (3×2%)</td>
</tr>
<tr>
<td>Elective Topic: Achievement of design objectives, as demonstrated in labs</td>
<td>Individual</td>
<td>10%</td>
</tr>
<tr>
<td>Elective Topic: Understanding of relevant subject material and individual contribution</td>
<td>Group</td>
<td>8%</td>
</tr>
<tr>
<td>Elective Topic: team performance</td>
<td>Group</td>
<td>3%</td>
</tr>
<tr>
<td>Elective Topic: Team report</td>
<td>Group</td>
<td>7%</td>
</tr>
</tbody>
</table>

## Deadlines:

Core topics Reflective task for are due on **Friday at 11pm** after the end of each topic (Fri W2, W4, and W7). Elective topic selection (with optional team formation preferences): **Week 7, Wednesday 11pm**. Elective topic report due: **Week 12, Wednesday 11pm**.

ELEC4123 – Term 1, 2020 – Course Outline
Page 3
COURSE DETAILS

Credits
This is a 6 UoC course. Since this course has no final examination, the workload of the course is compacted into just 10 weeks, so your effort must be adjusted accordingly. The expected average workload is 16 hours per week, which includes 8 hours of scheduled formal contact and 4 to 8 hours of independent study, design and preparation, including open labs and time spent working with peers. This is not only an expectation – it is a reality that most students undertaking this course do put in at least this amount of time!!

Relationship to Other Courses
This is a 4th-year course in the School of Electrical Engineering and Telecommunications, which is a core component of the BE and BE-ME programs (Electrical and Telecommunications) offered by the School.

This course directly ties into core courses in Electronics, Signal Processing, Control, Telecommunications, Data Networks and Energy and Power Systems which you should have already taken (typically in the third year of your program). See below for more on what is expected.

Pre-requisites and Assumed Knowledge
The course has three core topics, for which the following knowledge is assumed and crucially essential:

• Electronics (to the level of ELEC3106 (and partly ELEC2141 and ELEC2133)
• Signal Processing (to the level of ELEC3104)
• Control Systems (to the level of ELEC3114).

Through these and other courses, it is assumed that students have also developed good computer literacy and familiarity with MATLAB/Simulink, as well as microcontroller (Arduino in particular for Control Systems topic) which is used in some topics.

Learning outcomes
After successful completion of this course, you should be able to:

1. Have demonstrated an ability to work both individually and within a group, to produce designs which draw upon a number of disciplines previously studied in other courses.
   - The 4 design topics and 16 formal laboratory sessions all reinforce and assess these abilities.
2. Have demonstrated an ability to contribute to and learn from peers.
   - The elective design topic and interactive lectures all reinforce this ability, while the tutorial sessions both reinforce and assess it.
3. Have demonstrated a sufficient level of understanding and skill within a range of disciplines, together with an ability to explain design decisions.
   - The assessment methodology in laboratories deliberately reinforces and assesses these outcomes.

This course is designed to provide the above learning outcomes which arise from targeted graduate capabilities listed in Appendix A. The targeted graduate capabilities broadly support the UNSW and Faculty of Engineering graduate capabilities (listed in Appendix B). This course also addresses the Engineers Australia (National Accreditation Body) Stage I competency standard as outlined in Appendix C.

Syllabus
The course involves three core competency components, as follows:

• Electronic Circuit Design: Devices, amplifiers, tuned circuits, op-amp circuits, digital circuits, etc.
• Control System Design: Feedback and stability, linear control, data acquisition and sampling, etc.
• Signal Processing Design: Filter design, frequency response, spectrum analysis, BIBO analysis, etc.

The elective component of the course involves competency components in at least one of the following areas:

• Power System Design: Transformer, motor, power electronic converter, power factor, harmonics, etc.
• Networked Communications: Computer programming, socket programming, network protocols, distributed asynchronous systems, estimation and exploitation of local and system-wide timing information, etc.
• Physical Communications: Modulation schemes, robust detection of signals in noise, multiplexing and interference suppression, efficient bandwidth utilization, error control, etc.
• Analog Design: Power amplifiers for audio systems, analog filters, linear system design, etc.

Laboratory assessment requires the design, construction and understanding of working solutions to specified problems.

TEACHING STRATEGIES

Delivery Mode
The teaching in this subject is heavily focused on laboratories. Each of 4 design topics has 4 assigned laboratories, each 3 hours in duration, plus three optional open labs. The laboratories are designed to develop and assess proficiency. The majority of the assessment is individual, with a focus on objectively working solutions, in addition to understanding.

For the first 3 topics, the first 15min of the first lab of the week provide both input and an opportunity for class interaction using the video conferencing through all the lab rooms, albeit on a large scale.

Open labs are intended to provide an opportunity both to address knowledge gaps and also to reinforce an approach to design with more practical lab time, which focusses on the need to identify early what is most problematic about a design problem. Through this process, students are expected to be better prepared to approach the larger design problem that they will face as a team during the fourth (elective) design topic. To make sure that student won’t burnt out, the open lab times will be limited to maximum 4.5 hours for each open lab session during a week via booking time slots (total possible of 9hrs open lab). Students can book all the 4.5 hours in a row or book multiple time slots to avoid exhaustion and spending too much time in the lab as well as giving space to others to use the open lab.

At the end of each topic, there will be a catch-up lab for those who have been granted remarking a task or tasks of that topic due to legitimate reasons.

A very important aspect of the teaching in this course is the allocation of 12 hours in total to each topic plus plenty open lab times, which allows students to attempt design tasks multiple times and to learn from their mistakes between attempts. This strategy facilitates a reflective learning cycle.

Through these mechanisms, the course aims to build and ensure proficiency in the core areas of your program of study.

Due to the intensity and time pressure in this course for 10-week teaching system, as well as its coincidence with Thesis A/C seminars/poster presentations, two new no-lab weeks are incorporated into the course schedule. Week 5 is the first no-lab week allowing a cool-off period and catching up with the revisions for the upcoming topics. Week 9 is the second no-lab week which is mostly the Thesis A/C seminars/poster presentations week. This allows for students to have less stress about preparing for their thesis and the selected team for the elective topic can work in parallel on the design and testing during possibly arranged open labs in that week.

Design Topics
The course is divided into a sequence of three “core design topics” and one “elective design topic,” each of which is assigned four/4 formal laboratory sessions of 3 hours each.

The core design topics are:
  Topic 1: Electronic Circuits;
  Topic 2: Signal Processing; and
  Topic 3: Control Systems.

The elective topics are:
  Topic 4a: Energy Systems;
  Topic 4b: Data Networks; and
  Topic 4c: Telecommunications.
  Topic 4d: Analog Design
Each of the core topics consists of a sequence of design tasks, with progressively higher complexity. Design tasks for the core topics must be completed individually, although you are encouraged to discuss the topics with your fellow students outside the formal laboratory hours.

The elective design is performed in groups of at most 4 students. You must nominate which of the elective topics you intend to pursue by before the end of Week 7 (see the Indicative Laboratory Schedule on page 3), at which point you will also have an opportunity to propose a design team. If you are not part of a proposed team, or if unavoidable circumstances require it, you will be assigned to a team at the Course Convener’s discretion. You will be provided with further instructions on how to submit elective topic and team nominations. Unlike the first three design topics, the elective design is assessed only in the final week, however, the progressive observation of the team performance and individual contribution to the project is carried out by the lab demonstrators acting as tutors to help them better assess the teams in the final week.

Individual Learning
Preparation for labs is essential to success in this course. You should find yourself revising material from previous courses, discussing problems with your peers, raising questions in lectures, and perhaps struggling to find and solve problems you encounter with your design or implementation in the laboratory. All of these are outstanding learning opportunities.

Group Learning
You are strongly encouraged to discuss the design tasks with your classmates outside the laboratory sessions – laboratories themselves, however, are not the place for helping your friends or discussing design solutions, except during the elective topic.

The elective topic is a team effort, having larger scope and less incremental objectives than the first three design topics. To succeed in this topic, you will need to work effectively as a team member or leader. Moreover, each team is required to submit a report describing the design principles, implementation, outcomes and final reflections. The report will also need to be a team effort.

Laboratory Exemption
There is no laboratory exemption for this course. Regardless of whether equivalent labs have been completed in previous courses, all students enrolled in this course must take the labs. If, for medical reasons, (note that a valid medical certificate must be provided) you are unable to attend a lab, you will need to seek permission from the course convener to be assessed in a subsequent week.

ASSESSMENT

Assessment of core design tasks
All completed tasks for the three core design topics are to be assessed during the scheduled laboratory sessions by one of the laboratory demonstrators. Once you have completed a task, you should add your name to a list maintained by the demonstrators in your laboratory, so that you can be assessed as quickly as possible. You cannot expect to be assessed for all of the tasks you have completed during the final laboratory session of the topic, since this can place an unacceptable burden on the demonstrators’ time. As a result, we devised a plan for task assessment as follows:

- First lab session: At least one task is recommended to be completed and assessed (no more than two tasks will be assessed).
- For the next two lab sessions: At least one task must be completed and assessed, two tasks are recommended to be completed and assessed, but no more than two tasks will be marked.
- Open lab sessions: No assessments will be done during open labs. It is recommended that you work on your designs for at least two tasks during each open lab so that you can quickly get assessed in the next scheduled lab.
- Final assessment lab session: No more than two tasks will be assessed. So please make sure to not leave your tasks pile up for the final lab sessions.

Important note: You must at least complete three tasks from each topic with “satisfactory” grade to achieve a passing mark from that topic. The task grading system will be explained in the lecture.
Of the 24% of the overall course assessment that is associated with each core design topic, 12% is awarded based on actual outcomes. You cannot expect to obtain any of these marks for a solution which does not actually work or achieve the task objectives to some extent. 10% of the topic mark is awarded for your understanding of the design problem and your own design. To obtain these marks, you will need to convince the marker (one of the lab demonstrators) that you thoroughly understand your design and why you have selected it. Please note that your understanding mark will be usually capped to the achievement-of-the-requirements mark, but in some exceptional cases, it could slightly be higher.

At the end of each topic, you must submit a short reflective task worth 2% by answering to some questions to reflect on your work and learning gained from that topic. The submission of this task is through Moodle and the deadline is on the Sunday of the week before the next topic (e.g., Friday of Week 2 for Topic 1, Friday of Week 4 for Topic 2, and Friday of Week 7 for Topic 3). The mark is awarded for your genuine effort in providing your reflections on your work on each topic (there is no right or wrong answer to the question).

Assessment is individual. You may not present a group design or implementation for assessment within the core design topics. You MUST maintain a lab book for recording your observations as your marks will be written in your lab book and signed off by the marker. A lab book is an A4 size notebook containing a mix of plain pages and graph sheets. You have to purchase your own lab book from any stores.

Assessment of the elective design tasks
The elective design topic is a group activity, for which all final assessment will take place on Monday of week 11, but your team performance and individual contribution will be observed continuously by an allocated lab demonstrator to your group in the lab sessions. 28% of the overall course mark is allocated to the elective topic, 18% of which is awarded by the lab demonstrators in Week 10. 8% is awarded based on an individual interview of each team member, to determine their level of understanding of both the overall design and their individual contribution to it. The other 10% is awarded based on objective performance of the final design, a component of which will be competitive, meaning that teams will be ranked within each topic, based on the objective performance of their designs.

Each team will have a dedicated tutor/mentor. They will be circulating between their assigned teams to observe their interaction and thought processes, and to offer suggestions where appropriate. Your tutor will be especially interested in the way in which you approach the design problem, how you ensure that you focus on the most challenging parts of the problem first, how you reach an overall design that is likely to work, and how your team manages the resources at its disposal. Your tutor will also observe how individuals contribute to the team’s deliberations, design and interaction during elective topic scheduled lab sessions. Based on these observations, the tutor will award team performance mark worth 3% and your individual contribution with understanding which was mentioned in the previous paragraph (8%) which is a continuous assessment process.

Your team’s final report for the elective topic is an essential part of the reflective process worth 7%. You will be expected to have a preliminary version of the report available during the laboratory assessment exercise in Week 11. However, the report should be finalized afterwards, including a reflection on the design process that you followed, in light of your design’s performance. The report submission is due on Wednesday of Week 12.

Relationship of Assessment Methods to Learning Outcomes

<table>
<thead>
<tr>
<th>Assessment</th>
<th>Learning outcomes</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
</tr>
<tr>
<td>Core design tasks</td>
<td>✓</td>
</tr>
<tr>
<td>Elective design topic</td>
<td>✓</td>
</tr>
<tr>
<td>Elective design group report</td>
<td>✓</td>
</tr>
</tbody>
</table>
Mid-Semester Exam and Final Exam

There is no Mid-Semester exam or Final exam in this course.

COURSE RESOURCES

Textbooks

There are no specific texts for this course, but you should consider your lecture notes and text books from earlier classes in Electronics, Signal Processing, Control, Telecommunications, Data Networks and/or Energy Systems to be useful resources.

On-line resources

Moodle

As a part of the teaching component, Moodle will be used to disseminate teaching materials, host forums and occasionally quizzes. Assessment marks will also be made available via Moodle: https://moodle.telt.unsw.edu.au/login/index.php.

Mailing list

Announcements concerning course information will be given in the lectures and/or on Moodle and/or via email (which will be sent to your student email address).

OTHER MATTERS

Dates to note

Important Dates available at: https://student.unsw.edu.au/dates

Academic Honesty and Plagiarism

Plagiarism is the unacknowledged use of other people’s work, including the copying of assignment works and laboratory results from other students. Plagiarism is considered a form of academic misconduct, and the University has very strict rules that include some severe penalties. For UNSW policies, penalties and information to help you avoid plagiarism, see https://student.unsw.edu.au/plagiarism. To find out if you understand plagiarism correctly, try this short quiz: https://student.unsw.edu.au/plagiarism-quiz.

Student Responsibilities and Conduct

Students are expected to be familiar with and adhere to all UNSW policies (see https://student.unsw.edu.au/guide), and particular attention is drawn to the following:

Workload

It is expected that you will spend at least 15 hours per week studying a 6 UoC course, from Week 1 until the final assessment, including both face-to-face classes and independent, self-directed study. In periods where you need to complete assignments or prepare for examinations, the workload may be greater. Over-commitment has been a common source of failure for many students. You should take the required workload into account when planning how to balance study with employment and other activities.

Attendance

Regular and punctual attendance at all classes is expected. UNSW regulations state that if students attend less than 80% of scheduled classes they may be refused final assessment.

General Conduct and Behaviour

Consideration and respect for the needs of your fellow students and teaching staff is an expectation. Conduct which unduly disrupts or interferes with a class is not acceptable and students may be asked to leave the class.
Work Health and Safety
UNSW policy requires each person to work safely and responsibly, in order to avoid personal injury and to protect the safety of others.

Special Consideration and Supplementary Examinations
You must submit all assignments and attend all examinations scheduled for your course. You can apply for special consideration when illness or other circumstances beyond your control interfere with an assessment performance. If you need to submit an application for special consideration for an exam or assessment, you must submit the application prior to the start of the exam or before the assessment is submitted, except where illness or misadventure prevent you from doing so. Be aware of the “fit to sit/submit” rule which means that if you sit an exam or submit an assignment, you are declaring yourself well enough to do so and cannot later apply for Special Consideration. For more information and how to apply, see https://student.unsw.edu.au/special-consideration.

Continual Course Improvement
This course is under constant revision in order to improve the learning outcomes for all students. Please forward any feedback (positive or negative) on the course to the course convener or via the online student survey myExperience. You can also provide feedback to ELSOC who will raise your concerns at student focus group meetings. As a result of previous feedback obtained for this course and in our efforts to provide a rich and meaningful learning experience, we have continued to evaluate and modify our delivery and assessment methods.

New Changes: In this current version of the course, the assessment weights have been modified to make room for reflective tasks as both formative and summative assessment to better support the learning outcome in core topics. Also, the qualitative grading system has been introduced for marking to remove the stress from students and eliminate mark-driven assessment style. The mapping to numerical marks is then carried out by the course coordinator according to the rubric. Finally, a new schedule has been devised for the course due to the feedback from students on the intensity and time pressure in the course fooling the trimester teaching system. In this new schedule, there will be 4 official 3-hour lab sessions for every topic in two weeks (one hour less from previous offering of this course) plus two full-day open lab every week (of which the last acts as catch-up lab). This new plan allows to accommodate two no-lab weeks as cooling off weeks, one in Week 5 for preparation for the next upcoming topics and one in Week 9 for Thesis A/C seminar/poster presentations which is usually scheduled in that week. These no-lab weeks provide students with less stress about their Thesis as well as helping them with their mental health and wellbeing.

Administrative Matters
On issues and procedures regarding such matters as special needs, equity and diversity, occupational health and safety, enrolment, rights, and general expectations of students, please refer to the School and UNSW policies: https://student.unsw.edu.au/guide https://www.engineering.unsw.edu.au/electrical-engineering/resources

APPENDICES

Appendix A: Targeted Graduate Capabilities
Electrical Engineering and Telecommunications programs are designed to address the following targeted capabilities which were developed by the school in conjunction with the requirements of professional and industry bodies:

- The ability to apply knowledge of basic science and fundamental technologies;
- The skills to communicate effectively, not only with engineers but also with the wider community;
- The capability to undertake challenging analysis and design problems and find optimal solutions;
- Expertise in decomposing a problem into its constituent parts, and in defining the scope of each part;
- A working knowledge of how to locate required information and use information resources to their maximum advantage;
- Proficiency in developing and implementing project plans, investigating alternative solutions, and critically evaluating differing strategies;
• An understanding of the social, cultural and global responsibilities of the professional engineer;
• The ability to work effectively as an individual or in a team;
• An understanding of professional and ethical responsibilities;
• The ability to engage in lifelong independent and reflective learning.

Appendix B: UNSW Graduate Capabilities

The course delivery methods and course content directly or indirectly addresses a number of core UNSW graduate capabilities, as follows:

• Developing rigorous analysis, critique, and reflection, and ability to apply knowledge and skills to solving problems. These will be achieved by the laboratory experiments and interactive checkpoint assessments and lab exams during the labs.
• Developing ethical practitioners who are collaborative and effective team workers, through group activities, seminars and tutorials.
• Developing independent, self-directed professionals who are enterprising, innovative, creative and responsive to change, through challenging design and project tasks.

Appendix C: Engineers Australia (EA) Professional Engineer Competency Standard

<table>
<thead>
<tr>
<th>Program Intended Learning Outcomes</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>PE1: Knowledge and Skill Base</strong></td>
</tr>
<tr>
<td>PE1.1 Comprehensive, theory-based understanding of underpinning fundamentals</td>
</tr>
<tr>
<td>PE1.2 Conceptual understanding of underpinning maths, analysis, statistics, computing</td>
</tr>
<tr>
<td>PE1.3 In-depth understanding of specialist bodies of knowledge</td>
</tr>
<tr>
<td>PE1.4 Discernment of knowledge development and research directions</td>
</tr>
<tr>
<td>PE1.5 Knowledge of engineering design practice</td>
</tr>
<tr>
<td>PE1.6 Understanding of scope, principles, norms, accountabilities of sustainable engineering practice</td>
</tr>
<tr>
<td><strong>PE2: Engineering Application</strong></td>
</tr>
<tr>
<td>PE2.1 Application of established engineering methods to complex problem solving</td>
</tr>
<tr>
<td>PE2.2 Fluent application of engineering techniques, tools and resources</td>
</tr>
<tr>
<td>PE2.3 Application of systematic engineering synthesis and design processes</td>
</tr>
<tr>
<td>PE2.4 Application of systematic approaches to the conduct and management of engineering projects</td>
</tr>
<tr>
<td><strong>PE3: Professional and Personal Attributes</strong></td>
</tr>
<tr>
<td>PE3.1 Ethical conduct and professional accountability</td>
</tr>
<tr>
<td>PE3.2 Effective oral and written communication (professional and lay domains)</td>
</tr>
<tr>
<td>PE3.3 Creative, innovative and pro-active demeanour</td>
</tr>
<tr>
<td>PE3.4 Professional use and management of information</td>
</tr>
<tr>
<td>PE3.5 Orderly management of self, and professional conduct</td>
</tr>
<tr>
<td>PE3.6 Effective team membership and team leadership</td>
</tr>
</tbody>
</table>